

NanoArc ACE Mira RevA

Single-Sheet KiCad Pinmap Tables

A table-first wiring reference for drawing the low-voltage ACE controller schematic in KiCad 6

This PDF maps the RevA ACE controller parts to nets, pull-ups, pull-downs, decoupling, and test headers. Use it as a checklist while building one large KiCad schematic sheet. It is deliberately limited to the low-voltage controller, panel, analog simulator, fault simulator, and logic-only machine-I/O loopback.

Do not use this document as an output-stage construction plan. Nets such as PULSE_CMD, CHARGE_ENABLE, BLEED_ENABLE, and machine I/O are shown only as low-voltage test-header or simulator signals.

0. Global rules and resistor conventions

Item	KiCad net / use	Default value / implementation
Logic rail	+5V_LOGIC	5 V controller rail only. Add 100 uF at carrier input and 10 uF per module/branch.
Ground	GND	Logic ground only. Do not treat this as a high-current return.
I2C pull-ups	R_SDA, R_SCL	4.7 kOhm to +5V_LOGIC, one pair on the ACE carrier.
Switch inputs	Active-low switch nets	10 kOhm pull-up to +5V_LOGIC, switch/jumper closes to GND. Internal pullups are acceptable for first breadboard tests.
Command/test outputs	PULSE_CMD, CHARGE_ENABLE, BLEED_ENABLE	100 kOhm pulldown at exposed test connector/fixture so reset defaults low.
Talkback LEDs	D1-D8	+5V_LOGIC -> 1 kOhm -> LED anode -> LED cathode -> ULN2803 output.
IC decoupling	C_Ux	100 nF ceramic directly from each IC VDD/VCC pin to GND.
Unused CMOS input	Any unused 74HC/CMOS input	Tie to a defined rail or use 100 kOhm to a default rail. Never float.
Single-sheet schematic style	All long nets	Use labels, not long wires. Draw rectangles around functional blocks.

1. Reference designator map

Ref	Part	Circuit role	Footprint / KiCad treatment
U1	Arduino Nano Every ABX00028	ACE controller brain: direct inputs, I2C, SPI, serial diagnostics.	Draw as Nano module or two 1x15 headers/sockets.
J1/J2	Samtec SSW-115 socket strips	Removable Nano Every sockets.	PinSocket_1x15_P2.54mm_Vertical x2.
U2	Adafruit 1895 I2C FRAM breakout	Persistent storage module.	Use generated MOD_Adafruit_FRAM_1895_I2C symbol/footprint.
U3	MCP23017-E/SP	Panel input expander at 0x20.	DIP-28 socket.
U4	MCP23017-E/SP	Panel output expander at 0x21.	DIP-28 socket.
U5	MCP23017-E/SP	Machine I/O / low-voltage loopback expander at 0x22.	DIP-28 socket.
U6	MCP3208-CI/P	8-channel SPI ADC for analog simulators.	DIP-16 socket.
U7	REF5025AID	2.5 V ADC reference.	SOIC-8 to DIP-8 adapter.
U8	MCP6004-I/P	Quad op-amp buffer/filter for analog simulator channels.	DIP-14 socket.
U9	ULN2803A	Low-side driver for LEDs/buzzer.	DIP-18 socket.
U10	SN74HC573AN	Fault-source latch/diagnostic capture.	DIP-20 socket.
U11	CD74HC221E	Low-voltage timing/window test fixture.	DIP-16 socket.
U12-U14	LMV393IDR	Comparator channels for threshold/fault simulation.	SOIC-8 to DIP-8 adapters.
D1-D8	3 mm white LEDs	Talkback indicators.	LED_D3.0mm.
BZ1	PUI 5 V buzzer	Audible feedback.	12 mm buzzer footprint; verify pin pitch.
SW1-SW20	TL1105 tactile switches	4x5 keypad matrix.	6 mm pushbutton or exact TL1105 footprint.
ENC1	PEC11R encoder	Rotary input plus push switch.	PEC11R footprint or generic encoder switch.

2. U1 Arduino Nano Every direct pin map

U1 pin	Net	Dir	Connects to	Resistor/default	Note
D0/RX	UART_RX	In	Service UART/USB serial	Reserved; no external pull	Serial debug while OLED deferred.
D1/TX	UART_TX	Out	Service UART/USB serial	Reserved; no external pull	Do not spend on panel I/O.
D2	FAULT_SUM	In	Fault aggregation node	10 kOhm pull-up to +5V; active LOW	Direct critical summary.
D3	TRIP_OV	In	U12A comparator/latch output	10 kOhm pull-up if open collector; active LOW	Over-limit simulator.
D4	ARM_SW	In	ARM toggle to GND	10 kOhm pull-up to +5V; active LOW	Direct panel control.
D5	HARD_SAFE_SW	In	Hard safe switch to GND	10 kOhm pull-up to +5V; active LOW	Do not put behind I2C.
D6	GRIP_SW	In	Grip simulator switch/jumper to GND	10 kOhm pull-up to +5V; active LOW	Bench simulator.
D7	TRIGGER_SW	In	Trigger simulator switch/jumper to GND	10 kOhm pull-up to +5V; active LOW	Bench simulator.
D8	OUTPUT_FB	In	Low-voltage feedback simulator	10 kOhm pulldown if source can float	No energized output feedback.
D9	PULSE_CMD	Out	Test LED/header or U11 monostable input only	100 kOhm pulldown at fixture; optional 1 k series	No energy-stage connection in RevA KiCad.
D10	ADC_CS	Out	U6 pin 10 CS/SHDN	10 kOhm pull-up optional	SPI chip select.
D11	SPI_MOSI	Out	U6 pin 11 DIN	Optional 100 Ohm series	SPI data to ADC.
D12	SPI_MISO	In	U6 pin 12 DOUT	No pull normally	SPI data from ADC.
D13	SPI_SCK	Out	U6 pin 13 CLK	Optional 100 Ohm series	SPI clock.
A0	HW_INHIBIT	Out	Low-voltage inhibit/test header	100 kOhm pulldown at fixture	Safe-default low.
A1	CHARGE_ENABLE	Out	Test LED/header only	100 kOhm pulldown; 1 k LED resistor if used	Simulator only.
A2	ENCLOSURE_INTLK	In	Interlock jumper to GND	10 kOhm pull-up to +5V; active LOW	Direct interlock.
A3	EXPANDER_INT	In	U3/U4/U5 INTA if open-drain	10 kOhm pull-up to +5V; active LOW	Do not tie push-pull INTs together.
A4	I2C_SDA	Bi	U2 SDA; U3/U4/U5 pin 13	4.7 kOhm pull-up to +5V	Shared I2C bus.
A5	I2C_SCL	Out	U2 SCL; U3/U4/U5 pin 12	4.7 kOhm pull-up to +5V	Shared I2C bus.
A6	HANDPIECE_PRESENT	In	Presence jumper/header	10 kOhm pull-up; jumper to GND active LOW	Bench presence sim.
A7	TRIP_OC	In	U12B comparator/latch output	10 kOhm pull-up if open collector; active LOW	Over-current simulator.

3. I2C backbone and U2 FRAM breakout

From	Net	To	Resistor/part	Default/note
U1 A4	I2C_SDA	U2 SDA; U3 pin 13; U4 pin 13; U5 pin 13	R_SDA = 4.7 kOhm to +5V_LOGIC	One bus pull-up pair.
U1 A5	I2C_SCL	U2 SCL; U3 pin 12; U4 pin 12; U5 pin 12	R_SCL = 4.7 kOhm to +5V_LOGIC	Keep wiring short.
U1 A3	EXPANDER_INT	U3/U4/U5 INTA pin 20	R_INT = 10 kOhm to +5V_LOGIC	Only common if open-drain configured.

3.1 FRAM pin map

U2 pin	Net	Connect to	Resistor/default	Note
1 VCC	+5V_LOGIC	Logic rail	100 nF local optional	Breakout supply.
2 GND	GND	Logic ground	None	Ground.
3 WP	FRAM_WP or GND	Tie to GND for writable RevA	100 kOhm pulldown optional if jumpered	Low = write allowed.
4 SCL	I2C_SCL	U1 A5 / bus	Bus pull-up	Shared.
5 SDA	I2C_SDA	U1 A4 / bus	Bus pull-up	Shared.
6 A2	GND	Address strap	Direct GND or 10 kOhm to GND	Default low.
7 A1	GND	Address strap	Direct GND or 10 kOhm to GND	Default low.
8 A0	GND	Address strap	Direct GND or 10 kOhm to GND	Default low.

4. MCP23017 common DIP-28 map and address straps

Pin	Name	U3 Panel In 0x20	U4 Panel Out 0x21	U5 Machine Sim 0x22	Resistor / note
1	GPB0	KEY_ROW3	OLED_RST / spare	BLEED_ENABLE	Role-specific I/O.
2	GPB1	ENC_A	BUZZER_DRV	FAN_ENABLE	Use internal pullups for inputs.
3	GPB2	ENC_B	LAMP_TEST	CONTACT_TEST_ENABLE	Role-specific I/O.
4	GPB3	ENC_SW	PANEL_DIM	FAULT_LATCH_RESET	Role-specific I/O.
5	GPB4	PANEL_PRESENT	SPARE_OUT0	MACHINE_SPARE0	Panel present: 10 k pull-up, jumper to GND.
6	GPB5	SPARE_IN0	SPARE_OUT1	MACHINE_SPARE1	Define if unused.
7	GPB6	SPARE_IN1	SPARE_OUT2	MACHINE_SPARE2	Define if unused.
8	GPB7	SPARE_IN2	SPARE_OUT3	MACHINE_SPARE3	Define if unused.
9	VDD	+5V_LOGIC	+5V_LOGIC	+5V_LOGIC	100 nF to pin 10.
10	VSS	GND	GND	GND	Ground.
11	NC	NC	NC	NC	Do not connect.
12	SCL	I2C_SCL	I2C_SCL	I2C_SCL	Shared bus.
13	SDA	I2C_SDA	I2C_SDA	I2C_SDA	Shared bus.
14	NC	NC	NC	NC	Do not connect.
15	A0	GND	+5V_LOGIC	GND	Address bit.
16	A1	GND	GND	+5V_LOGIC	Address bit.
17	A2	GND	GND	GND	Address bit.
18	RESET	+5V via 10 k	+5V via 10 k	+5V via 10 k	Optional reset jumper to GND.
19	INTB	NC/test	NC/test	NC/test	Leave unused first.
20	INTA	EXPANDER_INT	EXPANDER_INT	EXPANDER_INT	Open-drain common only.
21	GPA0	KEY_COL0	TB_SAFE_DRV	CHARGER_READY	Role-specific.
22	GPA1	KEY_COL1	TB_CHARGE_DRV	CHARGER_FAULT	Role-specific.
23	GPA2	KEY_COL2	TB_READY_DRV	BLEED_CONFIRM	Role-specific.
24	GPA3	KEY_COL3	TB_ARMED_DRV	FAN_TACH_OR_GOOD	Role-specific.
25	GPA4	KEY_COL4	TB_OUTPUT_DRV	AUX_INTERLOCK	Role-specific.
26	GPA5	KEY_ROW0	TB_FAULT_DRV	SERVICE_KEY	Role-specific.
27	GPA6	KEY_ROW1	TB_ENERGY_DRV	POWER_MODULE_PRESENT	Role-specific.
28	GPA7	KEY_ROW2	TB_OPR_ERR_DRV	FAULT_LATCH_VALID	Role-specific.

5. U3 panel input expander and key matrix

U3 pin/name	Net	Connects to	Resistor/default	Firmware mode
21 GPA0	KEY_COL0	Key column C0	None	Output idle HIGH, scan LOW.
22 GPA1	KEY_COL1	Key column C1	None	Output idle HIGH, scan LOW.
23 GPA2	KEY_COL2	Key column C2	None	Output idle HIGH, scan LOW.
24 GPA3	KEY_COL3	Key column C3	None	Output idle HIGH, scan LOW.
25 GPA4	KEY_COL4	Key column C4	None	Output idle HIGH, scan LOW.
26 GPA5	KEY_ROW0	Key row R0	Internal pull-up or 10 k to +5V	Input active LOW.
27 GPA6	KEY_ROW1	Key row R1	Internal pull-up or 10 k to +5V	Input active LOW.
28 GPA7	KEY_ROW2	Key row R2	Internal pull-up or 10 k to +5V	Input active LOW.
1 GPB0	KEY_ROW3	Key row R3	Internal pull-up or 10 k to +5V	Input active LOW.
2 GPB1	ENC_A	Encoder A	Internal pull-up; encoder common to GND	Debounced input.
3 GPB2	ENC_B	Encoder B	Internal pull-up; encoder common to GND	Debounced input.
4 GPB3	ENC_SW	Encoder push	Internal pull-up; switch to GND	Input active LOW.
5 GPB4	PANEL_PRESENT	Panel-present jumper	10 k pull-up; jumper to GND	Input active LOW.
6-8 GPB5-GPB7	SPARE_IN0..2	Spare test pads	100 k pulldown or internal pull-up	Defined state.

5.1 Key matrix switch-to-net table

Switch	Label	Row side	Column side	Note
SW1	VERB	KEY_ROW0	KEY_COL0	No diode for RevA; one key at a time.
SW2	NOUN	KEY_ROW0	KEY_COL1	
SW3	+	KEY_ROW0	KEY_COL2	
SW4	-	KEY_ROW0	KEY_COL3	
SW5	CLR	KEY_ROW0	KEY_COL4	
SW6	7	KEY_ROW1	KEY_COL0	
SW7	8	KEY_ROW1	KEY_COL1	
SW8	9	KEY_ROW1	KEY_COL2	
SW9	KEY REL	KEY_ROW1	KEY_COL3	
SW10	RSET	KEY_ROW1	KEY_COL4	
SW11	4	KEY_ROW2	KEY_COL0	
SW12	5	KEY_ROW2	KEY_COL1	
SW13	6	KEY_ROW2	KEY_COL2	
SW14	PRO	KEY_ROW2	KEY_COL3	
SW15	ENTR	KEY_ROW2	KEY_COL4	
SW16	1	KEY_ROW3	KEY_COL0	
SW17	2	KEY_ROW3	KEY_COL1	
SW18	3	KEY_ROW3	KEY_COL2	
SW19	0	KEY_ROW3	KEY_COL3	
SW20	SPARE	KEY_ROW3	KEY_COL4	

6. U4 panel output through U9 ULN2803A

Function	U4 pin/net	U9 input	U9 output	Load wiring	Resistor/note
SAFE	21 GPA0 / TB_SAFE_DRV	1 IN1	18 OUT1	+5V -> R1 -> D1 anode; D1 cathode -> OUT1	R1 = 1 kOhm.
CHARGE	22 GPA1 / TB_CHARGE_DRV	2 IN2	17 OUT2	+5V -> R2 -> D2 anode; D2 cathode -> OUT2	R2 = 1 kOhm.
READY	23 GPA2 / TB_READY_DRV	3 IN3	16 OUT3	+5V -> R3 -> D3 anode; D3 cathode -> OUT3	R3 = 1 kOhm.
ARMED	24 GPA3 / TB_ARMED_DRV	4 IN4	15 OUT4	+5V -> R4 -> D4 anode; D4 cathode -> OUT4	R4 = 1 kOhm.
OUTPUT	25 GPA4 / TB_OUTPUT_DRV	5 IN5	14 OUT5	+5V -> R5 -> D5 anode; D5 cathode -> OUT5	R5 = 1 kOhm.
FAULT	26 GPA5 / TB_FAULT_DRV	6 IN6	13 OUT6	+5V -> R6 -> D6 anode; D6 cathode -> OUT6	R6 = 1 kOhm.
ENERGY	27 GPA6 / TB_ENERGY_DRV	7 IN7	12 OUT7	+5V -> R7 -> D7 anode; D7 cathode -> OUT7	R7 = 1 kOhm.
OPR ERR	28 GPA7 / TB_OPR_ERR_DRV	8 IN8	11 OUT8	+5V -> R8 -> D8 anode; D8 cathode -> OUT8	R8 = 1 kOhm.
U9 supply	Pin 9 GND; pin 10 COM	-	-	Pin 9 to GND. Pin 10 COM to +5V only if using inductive loads.	For LEDs only, COM may be NC.

6.1 U4 non-lamp pins

U4 pin/name	Net	Connection	Default/note
1 GPB0	OLED_RST	Deferred OLED reset/test pad	Leave NC or 100 k pull-up until OLED bought.
2 GPB1	BUZZER_DRV	Buzzer low-side driver input if using separate transistor/ULN spare	If all ULN channels are LEDs, use a separate small driver for buzzer.
3 GPB2	LAMP_TEST	Optional firmware/test signal	Can stay NC in first bring-up.
4 GPB3	PANEL_DIM	Optional LED enable/dim signal	Can stay NC in first bring-up.
5-8 GPB4-GPB7	SPARE_OUT0..3	Test pads only	100 k pulldown at external fixture if exposed.

7. U6 MCP3208 ADC and analog simulator

U6 pin	Name	Net	Connects to	Resistor/filter	Note
1	CH0	AIN0_VBANK_SIM	Pot/simulator wiper	1 k series; 100 nF to GND optional	Simulated bank voltage only.
2	CH1	AIN1_VIN_AUX_SIM	Pot/simulator wiper	1 k series; 100 nF optional	Aux voltage sim.
3	CH2	AIN2_ICHG_MON_SIM	Pot/simulator wiper	1 k series; 100 nF optional	Charge-current sim.
4	CH3	AIN3_IOUT_MON_SIM	Pot/simulator wiper	1 k series; 100 nF optional	Output-current sim.
5	CH4	AIN4_TBANK_SIM	U8 OUTA through 1 k	100 nF optional	Temp sim.
6	CH5	AIN5_TSTAGE_SIM	U8 OUTB through 1 k	100 nF optional	Temp sim.
7	CH6	AIN6_TACE_SIM	U8 OUTC through 1 k	100 nF optional	Board temp sim.
8	CH7	AIN7_THAND_SIM	U8 OUTD through 1 k	100 nF optional	Handpiece temp sim.
9	DGND	GND	Ground	None	Tie AGND/DGND locally.
10	CS/SHDN	ADC_CS	U1 D10	10 k pull-up optional	Deselect at reset.
11	DIN	SPI_MOSI	U1 D11	100 Ohm series optional	SPI data in.
12	DOUT	SPI_MISO	U1 D12	No pull	SPI data out.
13	CLK	SPI_SCK	U1 D13	100 Ohm series optional	SPI clock.
14	AGND	GND	Ground	None	Tie to DGND locally.
15	VREF	VREF_2V5	U7 VOUT	100 nF to GND near pin	ADC reference.
16	VDD	+5V_LOGIC	Logic rail	100 nF to GND	Supply.

7.1 U7 REF5025 adapter pin map

U7 pin	Function	Net	Connects to	Part/value	Note
1	DNC/NC	NC	No connection	None	Leave open.
2	VIN	+5V_LOGIC	Logic rail	100 nF to GND	Input supply.
3	TEMP	REF_TEMP_TEST/NC	Optional test pad	None	Leave NC first.
4	GND	GND	Ground	None	Ground.
5	TRIM/NR	REF_NR/NC	Optional cap to GND	TBD per datasheet	Leave NC first if unsure.
6	VOUT	VREF_2V5	U6 pin 15; pot top rail	100 nF to GND	2.5 V reference.
7	DNC/NC	NC	No connection	None	Leave open.
8	DNC/NC	NC	No connection	None	Leave open.

8. U8 MCP6004 analog buffer allocation

U8 pin	Function	Net	Connects to	Resistor/cap	Note
1	OUTA	BUF_AIN4_TBANK	U6 CH4 through 1 k	100 nF ADC-side optional	Follower output.
2	INA-	BUF_A_NEG	Tie to OUTA	Direct feedback	Follower.
3	INA+	TBANK_DIV	Thermistor/pot divider wiper	Divider TBD	Input A.
4	VDD	+5V_LOGIC	Rail	100 nF to GND	Supply.
5	INB+	TSTAGE_DIV	Divider wiper	Divider TBD	Input B.
6	INB-	BUF_B_NEG	Tie to OUTB	Direct feedback	Follower.
7	OUTB	BUF_AIN5_TSTAGE	U6 CH5 through 1 k	100 nF optional	Follower output.
8	OUTC	BUF_AIN6_TACE	U6 CH6 through 1 k	100 nF optional	Follower output.
9	INC-	BUF_C_NEG	Tie to OUTC	Direct feedback	Follower.
10	INC+	TACE_DIV	Divider wiper	Divider TBD	Input C.
11	VSS	GND	Ground	None	Ground.
12	IND+	THAND_DIV	Divider wiper	Divider TBD	Input D.
13	IND-	BUF_D_NEG	Tie to OUTD	Direct feedback	Follower.
14	OUTD	BUF_AIN7_THAND	U6 CH7 through 1 k	100 nF optional	Follower output.

9. U12-U14 LMV393 comparator adapters

Pin	Function	Generic wiring	Resistor/default	Note
1	OUT A	To trip/fault net	10 k pull-up to +5V	Open-collector output.
2	IN A-	Threshold/reference input	From pot/reference divider	Depends on role.
3	IN A+	Measured/simulated input	From simulator node	Keep 0-5 V.
4	GND	Ground	None	Ground.
5	IN B+	Measured/simulated input	From simulator node	Second channel.
6	IN B-	Threshold/reference input	From pot/reference divider	Second threshold.
7	OUT B	To trip/fault net	10 k pull-up to +5V	Open-collector output.
8	VCC	+5V_LOGIC	100 nF to GND	Supply.

9.1 Comparator role table

Comparator	Output net	Destination	Pull-up	Input role	Note
U12A	TRIP_OV_N	U1 D3 TRIP_OV and U10 D0	10 k to +5V	AIN0_VBANK_SIM vs OV_THRESHOLD	Active LOW.
U12B	TRIP_OC_N	U1 A7 TRIP_OC and U10 D1	10 k to +5V	AIN3_IOUT_MON_SIM vs OC_THRESHOLD	Active LOW.
U13A	TRIP_TEMP_N	U10 D2 and optional FAULT_SUM	10 k to +5V	Temp simulator vs threshold	Active LOW.
U13B	FEEDBACK_MISMATCH_N	U10 D3 and optional FAULT_SUM	10 k to +5V	OUTPUT_FB vs expected test state	Low-voltage logic only.
U14A	AUX_FAULT0_N	U10 D4/test header	10 k to +5V	Spare threshold	Spare.
U14B	AUX_FAULT1_N	U10 D5/test header	10 k to +5V	Spare threshold	Spare.

10. U10 SN74HC573 fault latch

Pin	Name	Net	Connects to	Resistor/default	Note
1	/OE	LATCH_OE_N	Tie to GND or U5 control	100 k pulldown if fixed enabled	LOW enables outputs.
2	D0	LATCH_D0_TRIP_OV	TRIP_OV_N	Already pulled up	Fault bit 0.
3	D1	LATCH_D1_TRIP_OC	TRIP_OC_N	Already pulled up	Fault bit 1.
4	D2	LATCH_D2_TRIP_TEMP	TRIP_TEMP_N	Already pulled up	Fault bit 2.
5	D3	LATCH_D3_FB_MISMATCH	FEEDBACK_MISMATCH_N	Already pulled up	Fault bit 3.
6	D4	LATCH_D4_AUX0	AUX_FAULT0_N	10 k pull-up if jumper source	Spare.
7	D5	LATCH_D5_AUX1	AUX_FAULT1_N	10 k pull-up if jumper source	Spare.
8	D6	LATCH_D6_EXP_FAULT	Jumper/test source	100 k default	Optional.
9	D7	LATCH_D7_SPARE	Jumper/test source	100 k default	Spare.
10	GND	GND	Ground	None	Ground.
11	LE	FAULT_LATCH_LE	Fault-event strobe/test jumper	100 k pulldown default hold	HIGH captures D inputs.
12	Q7	FAULT_SRC7	U5 input/test LED	1 k if LED	Diagnostic.
13	Q6	FAULT_SRC6	U5 input/test LED	1 k if LED	Diagnostic.
14	Q5	FAULT_SRC5	U5 input/test LED	1 k if LED	Diagnostic.
15	Q4	FAULT_SRC4	U5 input/test LED	1 k if LED	Diagnostic.
16	Q3	FAULT_SRC3	U5 input/test LED	1 k if LED	Diagnostic.
17	Q2	FAULT_SRC2	U5 input/test LED	1 k if LED	Diagnostic.
18	Q1	FAULT_SRC1	U5 input/test LED	1 k if LED	Diagnostic.
19	Q0	FAULT_SRC0	U5 input/test LED	1 k if LED	Diagnostic.
20	VCC	+5V_LOGIC	Rail	100 nF to GND	Supply.

11. U11 CD74HC221 low-voltage timing/window fixture

Logic-only timing/test block. Timing R/C values are intentionally TBD. Keep outputs to test LEDs, latch inputs, or headers only.

Pin	Function	Net	Connects to	Resistor/cap	Note
1	1A	PULSE_CMD_EDGE_A	U1 D9 through test/edge network	TBD defined idle state	Low-voltage only.
2	1B	PULSE_CMD_EDGE_B	Trigger/enable network or +5V	10 k as trigger mode requires	Document trigger mode.
3	1R	PULSE_WINDOW_RESET_N	Reset jumper/HW inhibit logic	10 k pull-up; active LOW reset	LOW terminates/reset.
4	1Q	PULSE_WINDOW_Q	Test LED/header/latch input	1 k if LED	Window output.
5	/2Q	MONO2_Q_N_SPARE	NC/test	Define if used	Spare.
6	2CX	MONO2_CX	Timing cap node	TBD or NC	If unused, terminate inputs.
7	2CXRX	MONO2_RXCX	Timing R/C node	TBD or NC	Spare mono.
8	GND	GND	Ground	None	Ground.
9	2A	MONO2_A	Unused input termination	Tie HIGH/LOW	No floating CMOS input.
10	2B	MONO2_B	Unused input termination	Tie HIGH/LOW	No floating CMOS input.
11	2R	MONO2_RESET_N	Unused reset termination	10 k pull-up	Inactive reset.
12	2Q	MONO2_Q	NC/test	None	Spare.
13	/1Q	PULSE_WINDOW_Q_N	Latch input or FAULT_SUM diode network	1N4148/10 k network if used	Complement output.
14	1CX	MONO1_CX	Timing capacitor node	C_CLAMP_TBD	No final value in this doc.
15	1CXRX	MONO1_RXCX	Timing resistor/cap node	R_CLAMP_TBD	No final value in this doc.
16	VCC	+5V_LOGIC	Rail	100 nF to GND	Supply.

12. U5 machine I/O simulator - low voltage only

U5 pin/name	Net	Dir	RevA destination	Resistor/default	Note
21 GPA0	CHARGER_READY	In	Loopback jumper	10 k pull-up; jumper to GND	Simulated status.
22 GPA1	CHARGER_FAULT	In	Loopback jumper	10 k pull-up; jumper to GND	Simulated status.
23 GPA2	BLEED_CONFIRM	In	Loopback/test header	10 k pull-up or driven source	Simulated status.
24 GPA3	FAN_TACH_OR_GOOD	In	Jumper	10 k pull-up; jumper to GND	No fan required.
25 GPA4	AUX_INTERLOCK	In	Jumper	10 k pull-up; active LOW	Aux sim.
26 GPA5	SERVICE_KEY	In	Jumper/switch	10 k pull-up; active LOW	Service input.
27 GPA6	POWER_MODULE_PRESENT	In	Jumper	10 k pull-up; active LOW	Simulator only.
28 GPA7	FAULT_LATCH_VALID	In	U10/test source	10 k pull-up if jumper source	Diagnostic.
1 GPB0	BLEED_ENABLE	Out	Test LED/header	100 k pulldown; 1 k LED optional	Do not connect to real dump load.
2 GPB1	FAN_ENABLE	Out	Test LED/header	100 k pulldown; 1 k LED optional	Low-voltage test.
3 GPB2	CONTACT_TEST_ENABLE	Out	Test LED/header	100 k pulldown	Low-voltage test.
4 GPB3	FAULT_LATCH_RESET	Out	U10/reset network	100 k pulldown optional	Diagnostic control.
5-8 GPB4-GPB7	MACHINE_SPARE0..3	I/O	Test pads	100 k default if exposed	Spare.

13. Direct switch and test-header wiring

Ref/header	Net	U1 pin	Wiring	Resistor/default	Active state
SW_ARM	ARM_SW	D4	Switch to GND	10 k pull-up to +5V	LOW = active/request.
SW_HSAFE	HARD_SAFE_SW	D5	Switch to GND	10 k pull-up to +5V	LOW = closed/satisfied depending firmware.
SW_GRIP	GRIP_SW	D6	Switch/jumper to GND	10 k pull-up	LOW = held/present.
SW_TRIGGER	TRIGGER_SW	D7	Momentary to GND	10 k pull-up	LOW = pressed.
J_ENCLOSURE	ENCLOSURE_INTLK	A2	Jumper to GND	10 k pull-up	LOW = satisfied.
J_HANDPIECE	HANDPIECE_PRESENT	A6	Jumper to GND	10 k pull-up	LOW = present.
J_OUTPUT_FB	OUTPUT_FB	D8	Loopback/test fixture output	10 k pulldown if source floats	Defined by test routine.
J_PULSE_TEST	PULSE_CMD	D9	Test LED/U11 input only	100 k pulldown; 1 k LED series if used	HIGH = logic test command.
J_CHG_TEST	CHARGE_ENABLE	A1	Test LED/header only	100 k pulldown; 1 k LED series if used	HIGH = simulated enable.
J_HW_INHIBIT	HW_INHIBIT	A0	Low-voltage test header	100 k pulldown	Safe default low.

14. Protection, headers, and KiCad checklist

Part/ref	Location	Nets/pins	Populate now?	Note
D_TV51 SMBJ5.0A	Power entry/protection block	Cathode +5V_LOGIC, anode GND	Later/final carrier	Add schematic placeholder.
ESD1-ESD4 TPD4E05U06	Connector entries	I/O lines plus GND	PCB only	Tiny USON; do not breadboard.
J_I2C_SERVICE	I2C test header	+5V, GND, SDA, SCL	Yes	Useful for probing/scanner.
J_SPI_ADC	ADC/SPI test header	ADC_CS, MOSI, MISO, SCK, GND	Optional	Logic-analyzer access.
J_ANALOG_SIM	Analog simulator header	AIN0..AIN7, VREF_2V5, GND	Yes	Lets pots live off-board.
J_MACHINE_SIM	Machine loopback header	U5 machine I/O nets	Yes	Low-voltage only.

14.1 KiCad work checklist

Step	KiCad action	Pass condition
1	Set one large A2/A1 landscape schematic sheet.	All blocks fit without long wires.
2	Draw zones: Power, Nano, I2C, Panel In, Panel Out, ADC, Fault, Machine Sim.	Each zone clearly titled.
3	Place U1-U14 and main headers before wiring.	Reference designators match this PDF.
4	Add +5V_LOGIC, GND, VREF_2V5, decoupling caps.	Every IC has supply and 100 nF.
5	Wire I2C bus and address straps.	FRAM 0x50; MCPs 0x20, 0x21, 0x22.
6	Wire direct Nano pins exactly from Section 2.	Every direct input has a defined default.
7	Wire keypad matrix and encoder.	Rows/columns match switch table.
8	Wire ULN and LEDs.	Each LED has its own 1 k resistor.
9	Wire ADC/reference/simulators.	ADC inputs stay within 0-VREF range in simulator.
10	Place fault logic as low-voltage simulator only.	No high-current stage symbols.
11	Run ERC repeatedly.	Only intentional/annotated warnings remain.

15. Net label index and bring-up order

Group	Net labels
Power	+5V_LOGIC, GND, VREF_2V5, REF_NR
I2C	I2C_SDA, I2C_SCL, EXPANDER_INT
SPI	ADC_CS, SPI_MOSI, SPI_MISO, SPI_SCK
Direct	FAULT_SUM, TRIP_OV, TRIP_OC, ARM_SW, HARD_SAFE_SW, GRIP_SW, TRIGGER_SW, OUTPUT_FB, PULSE_CMD, HW_INHIBIT, CHARGE_ENABLE, ENCLOSURE_INTLK, HANDPIECE_PRESENT
Panel input	KEY_COL0..KEY_COL4, KEY_ROW0..KEY_ROW3, ENC_A, ENC_B, ENC_SW, PANEL_PRESENT
Panel output	TB_SAFE_DRV, TB_CHARGE_DRV, TB_READY_DRV, TB_ARMED_DRV, TB_OUTPUT_DRV, TB_FAULT_DRV, TB_ENERGY_DRV, TB_OPR_ERR_DRV, BUZZER_DRV, OLED_RST
Analog	AIN0_VBANK_SIM, AIN1_VIN_AUX_SIM, AIN2_ICHG_MON_SIM, AIN3_IOUT_MON_SIM, AIN4_TBANK_SIM, AIN5_TSTAGE_SIM, AIN6_TACE_SIM, AIN7_THAND_SIM
Fault	TRIP_OV_N, TRIP_OC_N, TRIP_TEMP_N, FEEDBACK_MISMATCH_N, AUX_FAULT0_N, AUX_FAULT1_N, FAULT_SRC0..FAULT_SRC7
Machine sim	CHARGER_READY, CHARGER_FAULT, BLEED_CONFIRM, FAN_TACH_OR_GOOD, AUX_INTERLOCK, SERVICE_KEY, POWER_MODULE_PRESENT, FAULT_LATCH_VALID, BLEED_ENABLE, FAN_ENABLE, CONTACT_TEST_ENABLE, FAULT_LATCH_RESET

15.1 Bench/KiCad bring-up order

Stage	Build/test	Expected result
1	Nano carrier + serial + direct inputs.	Stable serial output; switches read correctly.
2	I2C pullups + FRAM.	I2C scanner finds 0x50.
3	Add U3.	Scanner finds 0x20; keypad rows/cols work.
4	Add encoder.	A/B direction and push switch report correctly.
5	Add U4 + one ULN LED.	One talkback blinks.
6	Add all LEDs/buzzer driver.	Lamp/sounder test matches labels.
7	Add ADC/reference/pots.	ADC readings stable and bounded.
8	Add comparators/latch.	Forcing thresholds changes trip nets and latch bits.
9	Add U11 monostable fixture.	Logic-only window output works on test LED/header.
10	Add U5 machine sim.	Loopbacks read and outputs toggle as expected.

End of pinmap tables. If a future schematic changes a net name, make a new revision of this document before soldering.